THAT WHICH IS CLAIMED IS:

1. A high frequency signal source comprising:

a dielectric resonator oscillator having an output signal;

a mixer that receives the output signal from the dielectric resonator oscillator; and

a phase locked loop circuit having a voltage controlled oscillator with a predetermined tuning range and operatively connected to said mixer such that said mixer receives an output signal from the voltage controlled oscillator and sums the output frequencies from the dielectric resonator oscillator and voltage controlled oscillator for creating a summed output frequency, wherein a portion of the summed output frequency is fed as a coupled signal into the phase locked loop circuit that is phase locked to a reference signal to compensate for dielectric resonator oscillator frequency errors due to manufacturing and for any drift due to temperature changes or aging, wherein a higher output frequency accuracy with low phase noise is achieved without manual tuning and a portion of the tuning range of the voltage controlled oscillator compensates for any dielectric resonator oscillator initial frequency errors and drift over temperature and aging.

2. A high frequency signal source according to Claim 1, and further comprising a crystal reference oscillator operatively connected to the phase locked loop circuit for providing a stable reference signal thereto.

3. A high frequency signal source according to Claim 1, and further comprising a filter operatively connected to the mixer for filtering the summed output frequency and eliminating unused side bands.

4. A high frequency signal source according to Claim 1, wherein said filter further comprises a high side filter for filtering the upper side band of the summed output frequency and provides a final output signal, and a low side filter operatively connected to the phase locked loop circuit for filtering the lower side band of the summed output frequency to provide a coupled signal to the phase locked loop circuit.

5. A high frequency signal source according to Claim 1, and further comprising an amplifier operatively connected to said mixer for amplifying the summed output frequency.

6. A high frequency signal source according to Claim 1, and further comprising a divider circuit positioned within said phase locked loop circuit for dividing the coupled signal by a factor "N".

7. A high frequency signal source according to Claim 1, and further comprising a phase locked loop chip having registers that are programmed for dividing the coupled signal and reference signal by a divide ratio between "M" and "N", respectively.

8. A high frequency signal source according to Claim 7, and further comprising a microcontroller operatively connected to said phase locked loop chip for programming the divide ratio between "M" and "N".

9. A high frequency signal source comprising:

a dielectric resonator oscillator having a field effect transistor and an output signal;

a mixer that receives the output signal from the dielectric resonator oscillator;

a phase locked loop circuit having a phase locked loop chip and a voltage controlled oscillator with a predetermined tuning range and operatively connected to said mixer such that the mixer receives an output signal from the voltage controlled oscillator and sums the output signals for creating a summed output frequency, wherein a portion of the summed output frequency is fed as a coupled signal into the phase locked loop chip that is phase locked to a reference signal to compensate for dielectric resonator oscillator frequency errors due to manufacturing and for any drift due to temperature changes or aging, wherein a higher output frequency accuracy with low phase noise is achieved without manual tuning and a portion of the tuning range of the voltage controlled oscillator is used to compensate for any dielectric resonator oscillator initial frequency errors and drift over temperature and aging; and

a microcontroller operatively to said field effect transistor of the dielectric resonator oscillator and phase locked loop chip for determining a divide ratio between "M" and "N" for the coupled signal and reference signal respectively and adjusting gate bias on the field effect transistor.

10. A high frequency signal source according to Claim 9, and further comprising crystal reference oscillator operatively connected to the phase locked

loop chip for providing a stable reference signal thereto.

11. A high frequency signal source according to Claim 9, and further comprising a filter operatively connected to the mixer for filtering the summed output frequency and eliminating unused side band signals.

12. A high frequency signal source according to Claim 11, wherein said filter further comprises a high side filter for filtering the upper side band of the summed output frequency and providing a final output signal, and a low side filter operatively connected to the phase locked loop circuit for filtering the lower side band of the summed output frequency and providing a coupled signal to the phased lock loop chip.

13. A high frequency signal source according to Claim 9, and further comprising an amplifier operatively connected to said mixer for amplifying the summed output frequency.

14. A high frequency signal source according to Claim 9, and further comprising a divider circuit positioned within said phase locked loop circuit and connected to said phase locked loop chip for dividing the coupled signal by a factor "N".

15. A high frequency signal source according to Claim 9, wherein said phase locked loop chip includes registers that are programmed for dividing the coupled signal and reference signal by a divide ratio between "M" and "N", respectively.

16. A method of generating a high frequency signal comprising the steps of:

mixing an output signal generated from a dielectric resonator oscillator with an output signal from a voltage controlled oscillator having a predetermined tuning range and part of a phase locked loop circuit to sum the frequencies for creating a summed output frequency; and

coupling a portion of the summed output frequency as a coupled signal into the phase locked loop circuit that is phase locked to a reference signal to compensate for dielectric resonator oscillator frequency errors due to manufacturing and for any drift due to temperature changes or aging, wherein a higher output frequency accuracy with lower phase noise is achieved without manual tuning and a portion of the tuning range of the voltage controlled oscillator compensates for any dielectric resonator oscillator initial frequency errors and drift over temperature and aging.

17. A method according to Claim 16, and further comprising the step of filtering the summed output frequency before coupling to aid in eliminating unused side bands.

18. A method according to Claim 17, and further comprising the step of filtering the summed output frequency within a high side filter that filters the upper side band of the summed output frequency for providing a final output frequency and filtering the summed output frequency of the summed signal within a low side filter that filters the lower side band to provide a signal to the phased lock loop circuit.

19. A method according to Claim 17, and further comprising the step of filtering within a bandpass filter.

20. A method according to Claim 16, and further comprising the step of amplifying the signal before coupling.

21. A method according to Claim 16, and further comprising the step of dividing the coupled signal by a factor "N".

22. A method according to Claim 16, and further comprising the step of dividing the coupled signal within a divider circuit.

23. A method according to Claim 16, and further comprising the step of dividing the coupled signal within registers contained within a phase locked loop circuit chip.